Comparative Study of Different Log Domain Integrators

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Abstract – Low voltage linear circuits have limited dynamic range and so input signal should be kept several times less than the bias level to reduce the harmonic distortion. For higher dynamic range, large bias levels are needed that causes large power consumption. Therefore, log domain technique is employed which uses companding method to overcome the aforesaid problem. Companding technique compresses the input signal to be further processed and later the output signal is expanded back to obtain the output signal in proportional to the input. In this paper, log domain integrators using CMOS, floating-gate MOSFET (FGMOS) and quasi-floating-gate MOSFET (QFGMOS) have been discussed and their performance has been compared. The CMOS log domain integrator shows pass band gain of -0.5 dB with -3 dB frequency of 165.6 MHz while for FGMOS and QFGMOS based integrators, the pass band gains are -0.8 dB and -0.5 dB with -3 dB frequencies of 6.84 MHz and 153.08 MHz respectively. It has been found that QFGMOS log domain integrator shows better results as compared to FGMOS based log domain integrator in terms of power dissipation, input resistance, output resistance, -3 dB frequency and current gain. The behavior of these circuits has been verified through PSpice simulations using level 7 parameters in 0.13 µm technology obtained from TSMC with supply voltage of 1V.

Index Terms – Low voltage circuits, Log domain Integrator, Sub-threshold MOSFET, FGMOS, QFGMOS

1. INTRODUCTION

All modern electronic systems majorly comprising of digital processors require an interface with the natural world through analog circuits. It is because of the fact that nearly everything that we hear, perceive or observe in life is all analog in nature [1]. With the advent of the portable electronic and mobile communication systems, low voltage and low power mixed mode circuit design has gained importance. Further, the operation of systems like biological implantable devices, mobile phones and hand held multimedia terminals relies on battery as main source of power. Such systems require low voltage and low power dissipation so as to have reasonable battery life and light weight [2-3]. Log domain circuits have linear relationship between the input and the output signal despite the internal processing done non-linearly. Integrator is a fundamental building block of log domain circuits which basically implement an input-output linear system using non-linear components and work on translinear principle. These circuits were implemented using bipolar junction transistors (BJT) which is inherently nonlinear. Therefore, the nonlinear characteristics of BJT can be employed for efficient signal processing in log domain. Though BJTs offer higher transconductance and high frequency response but they are not much subjected to down scaling. Therefore, there is a need to design log domain integrators using MOSFETs that enables the resulting integrators to undergo down scaling and make them suitable for integration and micro power applications. As CMOS integrators are useful in the design of microelectronic communication systems such as cell phones, data communication, audio and video signal processing but lack of tunability and large value of threshold voltage limit their use in low voltage and low power regime. Analog circuits based on Metal Oxide Semiconductor Filed Effect Transistors (MOSFET) biased in the sub-threshold region have been proved to be an efficient alternative for log domain integrators thus resulting in micro power circuits [4- 7]. Floating-gate MOSFET (FGMOS) has advantage of threshold voltage tunability and has been employed in number of low voltage applications [8-10]. But its low gain, low output impedance, degraded frequency response and more chip area are some of its limitations which can further be overcame by quasi-floating-gate MOSFET (QFGMOS). In this paper CMOS, FGMOS and QFGMOS log domain integrators have been presented and their performance has been compared by using PSpice simulations using level 7 parameters in 0.13 µm technology obtained from TSMC with supply voltage of 1V.

2. CMOS LOG DOMAIN INTEGRATOR

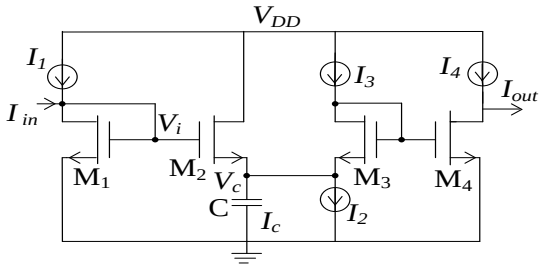

Figure 1 CMOS log domain integrator

The integrator is a fundamental unit of log domain circuits that employs the non linear behavior of MOSFET to realize linear functions. Without using linearization functions, log

domain circuits have simple structure and can operate at low voltage levels. It comprises of a translinear loop implemented by MOSFETs operating in weak inversion region and a grounded capacitor. CMOS log domain integrator is shown in figure 1 with all MOSFETs biased in sub-threshold region of operation [11].The circuit consists of NMOS transistors and grounded capacitor and thus is suitable for integration.

The drain current for n-channel MOSFET in sub-threshold region is given by [11]

$$I_{DS} = I_S e^{(1-n)\left(\frac{V_{BS}}{V_T}\right)} e^{\frac{nV_{GS}}{V_T}} \left(1 - e^{\frac{-V_{DS}}{V_T}} + \frac{V_{DS}}{V_o}\right) \quad (1)$$

where V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage, V_{BS} is the bulk-to-source voltage, I_S is the zero-bias current for the given device, $V_T = kT/q$ = 26mV at room temperature is the thermal voltage, V_o is the early voltage and n measures the effectiveness of the gate potential in controlling the channel current. For $V_{DS} \geq 4V_T$, assuming ideal V_o and ignoring the body effect, we have

$$I_{DS} = I_S e^{KV_{GS}} \quad (2)$$

where, $K = \frac{n}{V_T}$

Now, in figure 1 if we assume $I_1=I_2/2=I_3=I_4=I_o$

then expression for transfer function becomes

$$\frac{I_{out}(s)}{I_{in}(s)} = -\frac{1}{s\tau + 1} \quad (3)$$

where $\tau = C/(KI_o)$ is integrator time constant. The CMOS log domain integrator of figure 1 has been simulated using level 7 PSpice parameters for 0.13 µm technology with supply voltage of 1V and capacitance is 0.01 pF, bias current I_2=1µA, $I_1=I_3=I_4$=.5µA. The aspect ratio of MOSFETs is 2.6µm/.13µm for M1, 1.3µm /.13µm for M2 and M3, and .39µm /.13µm for M4. The resulting frequency response is shown in figure 2 which shows pass band gain of -0.5 dB with -3 dB frequency of 165.6 MHz.

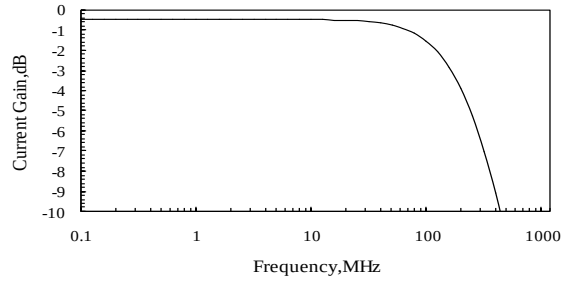

Figure 2 Frequency response of CMOS log domain integrator

3. FGMOS LOG DOMAIN INTEGRATOR

In order to improve the performance of CMOS log domain integrator in terms of low threshold voltage and bias dependent tunable characteristics, FGMOS log domain integrator has been designed as shown in Fig. 3. In FGMOS log domain integrator gate is floating therefore, the multi-inputs are capactively coupled to the floating gate and bias voltage is applied through large value capacitor (twice the input capacitor) to one of the input terminals so as to reduce the threshold voltage (V_{th}). Here, C_1 and C_2 are the coupling capacitors used for applying input signal and bias voltage respectively in M1 whereas C_3 and C_4 have similar function in M4. The threshold voltage reduces for the condition $C_2 >> C_1$ [12]. The circuit of FGMOS log domain integrator as shown in figure 3 has been simulated by choosing V_{b1} = 0.2V and V_{b2}= 0.25V with the same values of aspect ratios, bias currents and other parameters as those of CMOS log domain integrator in figure 1. The simulated frequency response is shown in figure 4 which shows a pass band gain of -0.8 dB with -3 dB frequency of 6.84MHz.

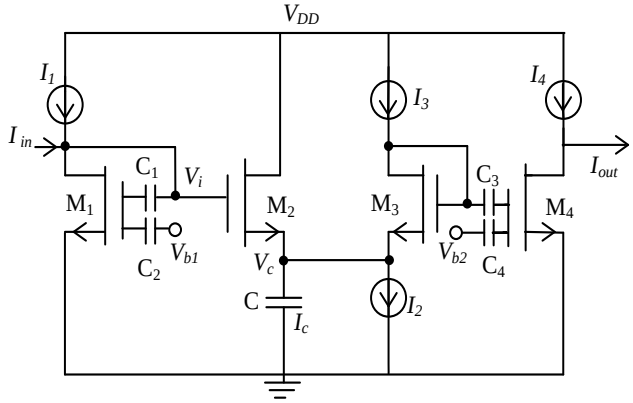

Figure 3 FGMOS log domain integrator

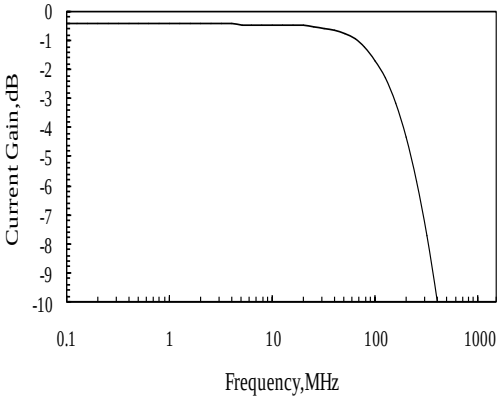

Figure 4 Frequency response of FGMOS log domain integrator

4. QFGMOS LOG DOMAIN INTEGRATOR

Since the structure of FGMOS incorporates a large bias capacitor for reducing threshold voltage, so there occurs degradation in frequency response restricting the application of resulting circuits at high frequency besides occupying more silicon area while actual implementation and reduced gain bandwidth product. In QFGMOS log domain integrator, the gate is not floating like in FGMOS log domain integrator but is weakly connected to one of the supply rails through a high value resistor implemented with reverse biased MOSFET of opposite type. Besides, lowering the supply voltage requirements, QFGMOS offers better frequency response and needs less chip area [13].

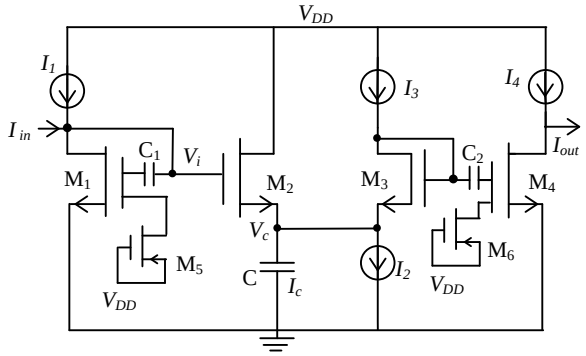

Figure 5 QFGMOS log domain integrator

The simulation results of QFGMOS log domain integrator has been obtained with same parameters as that of FGMOS log domain integrator with same values of bias current and all MOSFETs operating in sub-threshold region shows pass band gain of -0.5 dB with -3 dB frequency of 153.08MHz as shown in figure 6.

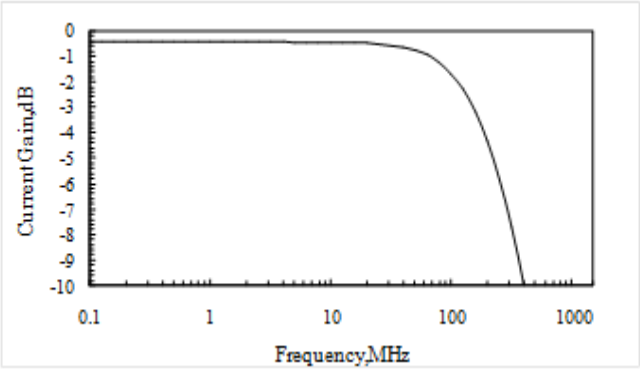

Figure 6 Frequency response of QFGMOS log domain integrator

The comparative frequency and phase responses of CMOS, FGMOS and QFGMOS log domain integrator is shown in figures 7 and 8 respectively which reveals that QFGMOS log domain integrator is better than others. Phase response shown variation of phase of output signal from 0 to -180 degrees.

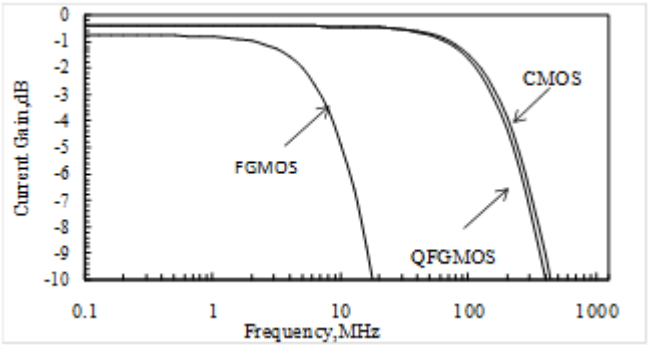

Figure 7 Comparative Frequency response of log domain integrator

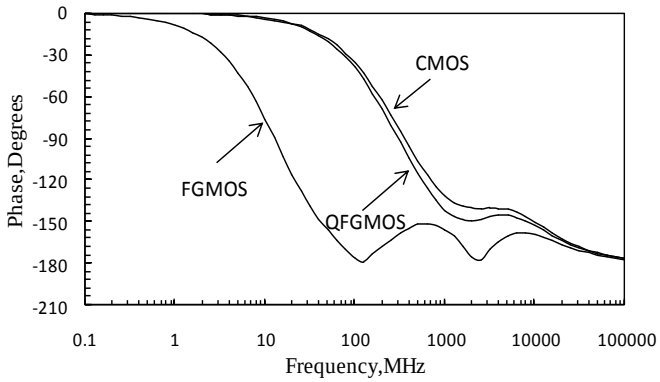

Figure 8 Comparative Phase response of log domain integrator

Parameters	CMOS	FGMOS	QFGMOS
Supply voltage	1V	1V	1V
Power dissipation	1.56 µw	1.68 µw	1.5 µw
Input Resistance	74 kΩ	206 kΩ	74.1 kΩ
Output resistance	1.81MΩ	1.49 MΩ	1.82 MΩ
Current Gain	-0.5dB	-0.8 dB	-0.5 dB
-3dB frequency	165.6 MHz	6.84 MHz	153.08 MHz

Table 1 Summary of results

Table 1 shows values of different parameters of different log domain integrators for comparative purpose such as supply

voltage, power dissipation, input resistance, output resistance, current gain and -3dBfrequency.

5. CONCLUSION

In this paper, we have presented the study of CMOS, FGMOS and QFGMOS log domain integrators wherein CMOS log domain integrator has been considered as prototype for other designs. The simulation results of CMOS log domain integrator shows pass band gain of -0.5 dB with -3 dB frequency of 165.6MHz. While FGMOS log domain integrator shows pass band gain of -0.8 dB with -3 dB frequency of 6.84MHz at same value of bias current. Further, QFGMOS log domain integrator has pass band gain of -0.5 dB with -3 dB frequency of 153.08MHz and the value of capacitor chosen is 0.01 pF. Comparison of frequency and phase response of all three topologies is also presented. It has been seen that QFGMOS has better performance as compared to other integrator topologies in terms of power dissipation, output resistance, and bandwidth. The behavior of these circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 μm CMOS technology obtained from TSMC with a supply voltage of 1V. The simulation results have been found to be close conformity with theoretical predictions.

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